Low Power Solutions in FPGA based Programmable Heterogeneous Systems

Dr. Yankin Tanurhan,
Actel Corporation, Mountain View
**Vice President, System Solutions and
Advanced Applications**

Overview

- **Why is power a problem ?**

- **What can FPGA's do ?**

- **Are we safe now ?**

- **What else can FPGA's do ?**

- **Summary**

The Shrink and Its Impact

- **Speed**

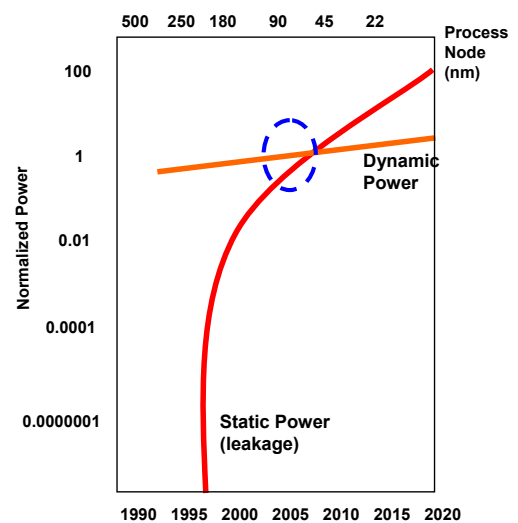- **Cost**

- **Power**

Semiconductor Industry Challenges

- **Static power increases significantly at <100nm geometries**

- **Subthreshold Leakage**
  - **Raising VT helps, but there's a limit.**
  - **Strain helps, but that's already been done**
  - **Worsens with reduced voltage**

- **Power and Speed at Odds**

- **Power is becoming a market limiter**

Source: Int'l Technology Roadmap
for Semiconductors (ITRS)
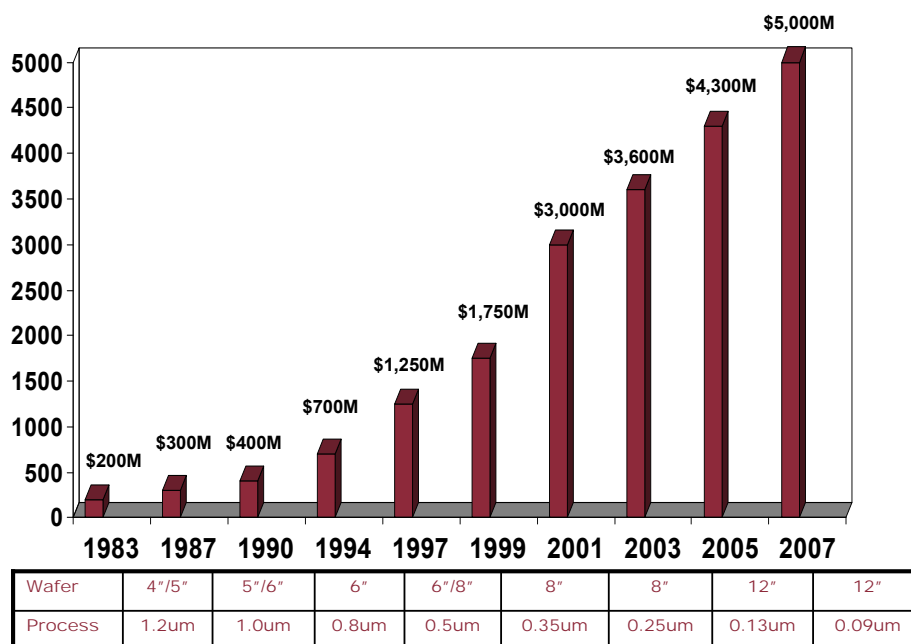
What about Dynamic Power

Power = CV²F

$$\text{Power} = CV^2F$$

C - Low K helps, but C is going up
    due to higher densities

V - Fell previously, but now same

F - Increasing steadily

Semiconductor Fab Cost Trend

Rising Fab Cost

Source: UMC

	1983	1987	1990	1994	1997	1999	2001	2003	2005	2007
Wafer	4"/5"	5"/6"	6"	6"/8"	8"	8"	12"	12"		
Process	1.2um	1.0um	0.8um	0.5um	0.35um	0.25um	0.13um	0.09um		

Chart values: $200M, $300M, $400M, $700M, $1,250M, $1,750M, $3,000M, $3,600M, $4,300M, $5,000M

Trends Continue to Drive Demand for Low-power FPGAs

Actel POWER MATTERS

- **Portable and battery-operated electronics proliferation**
- **Hyper-competitive markets with shorter product lifecycles and evolving standards**
  - **Increasing need for interfacing, bridging and control**
- **Power budgets tighten**
  - **Features, performance and complexity grow, but not at expense of draining the battery or increasing footprint**
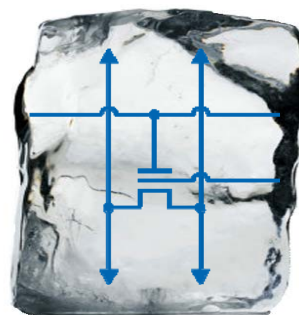- **Static power consumption and low-power modes most important for portables**

Flash's Fundamental Advantage

Actel POWER MATTERS

Typical Competitors SRAM Cell – 6T

Bit Line   Vdd   Vdd   Bit Line

Word Line
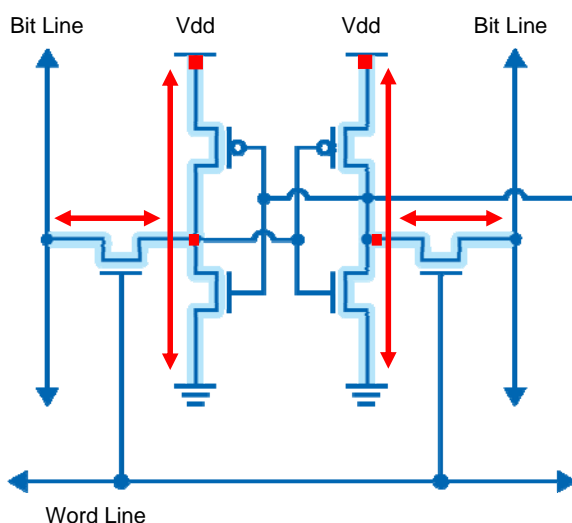
Actel
Flash Cell – 1T

- **Substantial Leakage per Cell**
- **High Static Current**

- **Negligible leakage per cell**
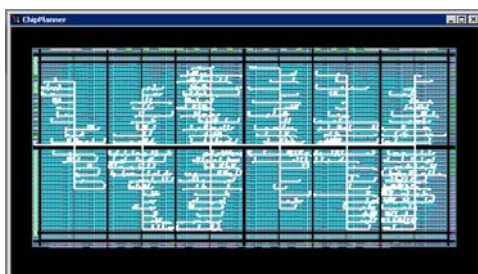- **Ultra Low Static Current**

What did we do in Technology and Design

- **Integrate Flash and High Speed embedded logic process**

- **Deploy Low Power Vt options, Multiple Threshholds**

- **Single supply for core and I/Os**
  - **As low as 1.2V**

- **Seamless Low Power Power modes**
  - **Static, Flash*Freeze**

- **Feature-Rich**
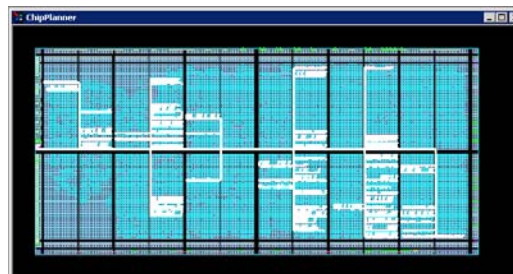 - **RAM, PLL, I/O Standards, Cortex-M1**

Power-Aware Tools

- **Power Driven Layout**
  - **Yields lowest power consumption possible**
  - **Reduces dynamic power by 30%**

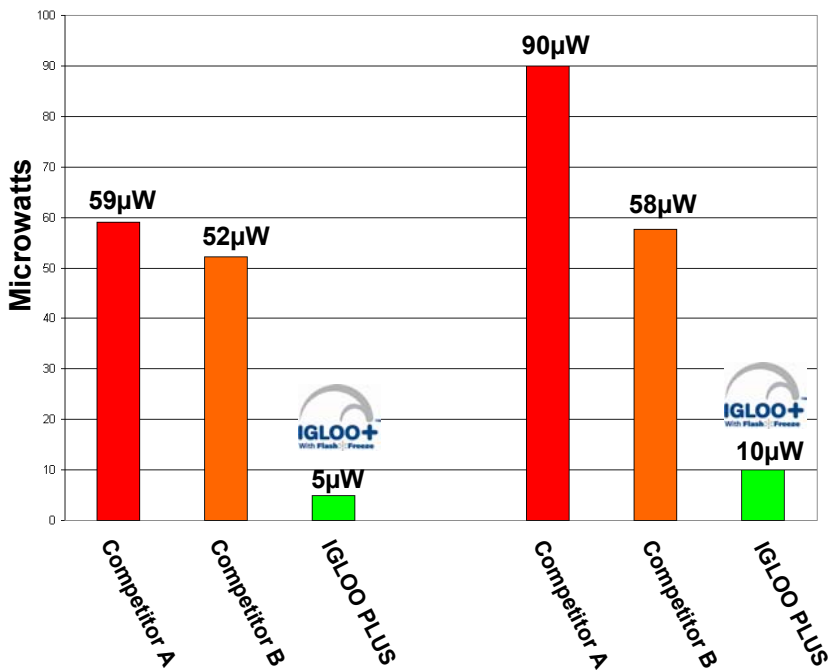**Timing-driven layout**   **Power-driven layout**

- **SmartPower**
  - **Create Power profiles based on functional modes**
  - **Cycle-accurate analysis**
  - **Spurious transitions analysis**
  - **Battery life estimation tool**
  - **Enable Variable Voltage use modes**
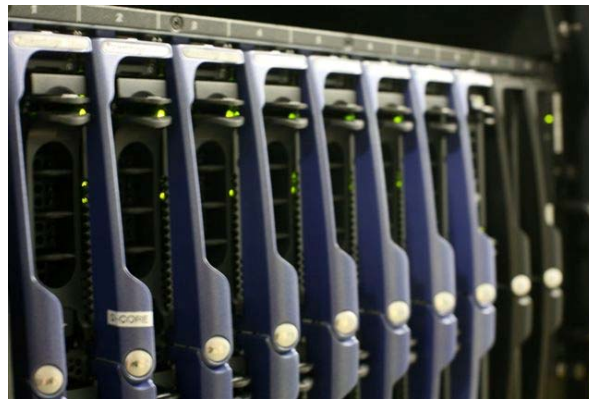
A Static Power Comparison

30k system gates

60k system gates

- **IGLOO PLUS 5µW**
- **Competitors**
  - "Low-power CPLDs"
  - SRAM-based, low-power PLDs
  - **10x higher power**

Declare victory and go home.

Server Room

Server Math

Power for:

100%	**Server**
60 %	**Fan and Air Conditioning**
60%	**Switch, Router and Network**
220%	

IE Total Power = 2.2x Server Power

Press Coverage: Server Farms

- **4 Google**
  - **2 North Carolina**
  - **1 South Carolina**
  - **1 Oregon**
- **1 MicroSoft – Washington**
- **1 Yahoo – Washington**

- **All close to cheap, plentiful power**

- **1.2% of electricity consumed in the US is used in server farms**

"Energy costs will soon eclipse hardware costs. Possibly by a large margin."

Luiz Barroso. Google

Industry is reacting with System Management Standards

- **Telecommunications Computing Architecture (TCA)**
  - **Standards by PCI Industrial Computer Manufacturers Group (PICMG)**
- **Advanced Telecommunications Computing Architecture (ATCA)**
  - **December 2002 PICMG standard**
  - **Current rev of std is PICMG 3.0 R2.0 ECN002 adopted 29 April 2006**
  - **Architecture for high-performance, high-density, packet-based systems**
- **Advanced Mezzanine Card (AMC)**
  - **January 2005 PICMG standard**
  - **Current rev of std is PICMG AMC.0 R2.0 adopted 15 November 06**
  - **Extends ATCA's high-bandwidth multi-protocol interface to hot-swappable modules for easy design, scaling, servicing**
- **MicroTCA (µTCA)**
  - **July 2006 PICMG standard**
  - **Current rev of std is PICMG MTCA.0 R1.0 adopted 06 July 2006**
  - **Smaller form-factor chassis delivers central power management, lower cost, high availability**
- **Intelligent Platform Management Interface (IPMI)**
  - **1995 standard initiated by Intel. Dell, HP, Intel and NEC announced IPMI v1.0 on 16 September 1998**
  - **Current rev of std is IPMI v2.0 rev. 1.0 specification markup for IPMI v2.0/v1.5 errata revision 3 dated 15 February 2006**
  - **Intelligent Platform Management Bus (IPMB) defines internal management bus for extending platform management within a chassis**
  - **Intelligent Chassis Management Bus (ICMB) defines external management bus between IPMI enabled systems**
- **ATCA, AMC, MicroTCA all communicate using IPMI protocol**

Our customers are in need of System Management

- **Manage Power Up: Power Sequencing, Status Monitoring**
- **Monitor Sensors and Report Status, Sensor Data**
  - Temperature
  - Voltage
  - Current
  - Boot Status
- **Take Immediate Actions based on Sensor Readings**
  - Over/undervoltage/current/temp
- **Communicate with System Controllers/Hubs**
  - Oversee system inventories
  - Implement system-level redundancy
  - Manage Hot Swap
  - Respond to management queries and commands

Summary

- **Power-conscious design is becoming more critical**
  - Not only choice of components but designing smart for power
- **You can minimize power consumption today**
  - Innovative low-power FPGAs and programmable system chips
  - Power optimization tools
- **At 5µW, Actel's IGLOO family is the low-power PLD leader**
- **We continue to expand our Power Concious FPGA portfolio with families like Fusion to adress power management needs**